Listing of Claims

1-30 (Canceled)

31. (Currently Amended) A semiconductor device, comprising:

a first set of signal wires, including a first plurality of signal wires distributed ~~among at least~~ in a first layer and a second plurality of signal wires distributed in a ~~and~~ second adjacent ~~layers~~ layer;

a second set of signal wires, including a third plurality of signals wires distributed ~~among at least~~ in the first layer and ~~second layers~~ a fourth plurality of signal wires distributed in the second layer, the first and second sets having a different number of signal wires, with the signal wires in the first set being substantially parallel and arranged in a first pattern, and the signal wires in the second set being substantially parallel and arranged in a second pattern.

32. (Previously Presented) The semiconductor device of claim 31, wherein each of the first and second sets have an even number of signal lines.

33. (Previously Presented) The semiconductor device of claim 31, wherein the first layer has a number of signal wires from the first and second sets different from a number of signal wires from the first and second sets in the second layer.

34. (Previously Presented) The semiconductor device of claim 31, wherein the first and second patterns are a same pattern.

35. (Canceled)

36. (Previously Presented) The semiconductor device of claim 31, wherein the first and second patterns are alternating patterns.

37. (Previously Presented) The semiconductor device of claim 31, wherein the number of signal wires in the first layer of the first set is different from the number of signal wires in the first layer of the second set.

38. (Canceled)

39. (Previously Presented) The semiconductor device of claim 31, wherein the first and second layers are adjoining layers.

40-47 (Canceled)

48. (Previously Presented) The semiconductor device of claim 31, wherein signal wires in the first layer are local interconnect wires and signal wires in the second layer are global routing wires.

49. (Previously Presented) The semiconductor device of claim 31, wherein the signal wires in the first set have a same permittivity and the signal wires in the second set have a same permittivity.

50. (Previously Presented) The semiconductor device of claim 31, wherein the first set of signal wires is separated from the second set of signal wires.

51. (Previously Presented) The semiconductor device of claim 50, wherein the first set of signal wires is separated from the second set of signal wires by one or more ground or return wires.

52. (Previously Presented) The semiconductor device of claim 51, wherein the first set of signal wires is separated from the second set of signal wires by ground or return wires in the first and second layers.

53. (Previously Presented) The semiconductor device of claim 52, wherein the first set of signal wires is located between the one or more ground or return wires and one or more power supply wires.

54. (Previously Presented) The semiconductor device 53, wherein the second set of signal wires is located between the one or more ground or return wires and one or more additional power supply lines.

55. (Previously Presented) The semiconductor device of claim 54, wherein the signal wires from the first and second sets located in the first layer are between first and second power supply lines in the first layer.

56. (Previously Presented) The semiconductor device of claim 55, wherein the signal wires from the first and second sets that are located in the second layer are between third and fourth power supply lines in the second layer.

57-64 (Canceled)

65. (New) The semiconductor device of claim 31, wherein the first layer is formed over the second layer.

66. (New) The semiconductor device of claim 31, wherein the signal lines in the first and second sets are oriented in a same direction.

67. (New) The semiconductor device of claim 31, wherein the signal lines in the first and second sets are parallel to one another.